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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,353	10/18/2000	James W. Adkisson	BUR9-1999-0300-US1	3972

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WHITHAM, CURTIS & CHRISTOFFERSON, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,353	ADKISSON ET AL.	
	Examiner	Art Unit	
	Khiem D Nguyen	2823	AW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *2-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 14-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 17th, 2003 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-30) are pending in the application in which claims 2-13 are withdrawn from consideration.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Neudeck et al. (U.S. Patent 5,273,921).

In re claim 1, **Neudeck** discloses a method of forming a field effect transistor (FET) transistor, comprising (col. 5, line 55 to col. 8, line 35 and **FIGS. 2A-3J**): providing a substrate **(FIGS. 3A-J: 40)**; forming a layer on the substrate, the layer having exposed side surfaces; forming an epitaxial channel **(FIG. 3D: 52A)** (col. 7, lines 42-55) on the each of the exposed side surfaces of the layer, the channel having an exposed first

sidewall **(FIG. 3E: 53)** opposite the layer **(FIG. 3D)**; removing a channel on a first side of the layer and then removing the layer **(FIG. 3F)** (col. 7, line 67 to col. 8, line 3), thereby exposing a second sidewall of the channel formed on the second side of the layer; forming a second channel in place of removed channel **(FIG. 3G: 57 and FIG. 3I: 57A)** (col. 8, lines 4-27); and forming a gate **(FIG. 3I: 62)** adjacent to at least one of the sidewalls **(FIG. 3I: 60)** of the channel and the second channel, there being a gate dielectric **(FIG. 3I: 61)** between each channel and the gate (col. 8, lines 28-35).

3. Claims 14-19, and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Neudeck et al. (U.S. patent 5,273,921).

In re claim 14, **Neudeck** discloses a method for forming a double gated field effect transistor (FET), comprising the steps of (col. 5, line 55 to col. 8, line 35 and **FIGS. 1A-3J)**: forming on a substrate **(FIG. 3D: 40)** a first and second epitaxially grown channels **(FIG. 3D: 52A)**, the channels having side surfaces extending up from the substrate, wherein the second channel **(FIG. 3G: 57 and FIG. 3I: 57A)** is grown following removal of a central semiconductor region upon which the first channel was grown (col. 7, line 67 to col. 8, line 27); etching areas within a silicon layer to form a source **(FIG. 3I: 58)** and a drain **(FIG. 3I: 59)**, wherein a side surfaces of the source and the drain contact opposing end surfaces of the first and second epitaxially grown channels; and forming a gate **(FIG. 3I: 42, 62)** that contacts a top surface and two side surfaces of the first and second epitaxially grown channels and a top surface of the substrate.

In re claim 15, **Neudeck** discloses wherein the forming step comprises the steps of: forming first and second semiconductor line, each end of the silicon lines contacting one of the source **(FIG. 3I: 58)** and the drain **(FIG. 3I: 59)**; forming an etch stop layer **(FIG. 3E: 53)** on an exposed side surface of each of the first and second semiconductor lines; epitaxially growing first and second semiconductor layers **(FIG. 3D: 52A)** on each etch stop layer; etching away the first and second semiconductor lines and the etch stop layers (col. 7, line 67 to col. 8, line 3); filling areas surrounding the first and second epitaxially grown semiconductor layers and between the source and the drain with an oxide fill **(FIG. 3E: 54)**; and etching a portion of the oxide fill to form an area that defines a gate **(FIG. 3I: 42, 62)**, wherein the area that defines the gate is substantially centered between and substantially parallel to the source and the drain (col. 8, lines 9-35);

In re claim 16, **Neudeck** discloses wherein the method as recited in claim 15, further comprising the steps of: etching the oxide fill between the gate the source to expose the first and second epitaxially grown silicon layers (col. 8, lines 4-8 and **FIG. 3G**); and etching the oxide fill between the gate **(FIGS. 3I: 42, 62)** and the drain **(FIG. 3I 59)** to expose the first and second epitaxially grown silicon layers.

In re claim 17, **Neudeck** discloses wherein the method as recited in claim 16, further comprising the step of forming an oxide **(FIG. 3H: 60)** on the first and second epitaxially grown silicon layers (col. 8, lines 8-35).

In re claim 18, **Neudeck** discloses wherein the oxide is silicon dioxide.

In re claim 19, **Neudeck** discloses wherein the method as recited in claim 14, further comprising the steps of: implanting a portion of the epitaxially grown silicon

layers between the gate **(FIG. 3I: 42, 62)** and the source **(FIG. 3I: 58)** (col. 8, lines 9-27); and implanting a portion of the epitaxially grown silicon layers between the gate and the drain **(FIG. 3I: 59)**.

In re claim 22, **Neudeck** discloses wherein the method as recited in claim 14, further comprising the step of forming a contact **(FIG. 3J: 63, 64)** on each of the gate **(FIG. 3J: 42, 62)**, the source **(FIG. 3J: 58)** and the drain **(FIG. 3J: 59)** (col. 8, lines 28-35).

In re claim 23, **Neudeck** discloses wherein the method as recited in claim 14, wherein the gate material is polysilicon (col. 8, lines 8-27).

4. Claims 24-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Neudeck et al. (U.S. patent 5,273,921).

In re claim 24, **Neudeck** discloses a method of forming an FET, comprising (col. 5, line 55 to col. 8, line 35 and **FIGS. 1A-3J**): forming on a substrate **(FIG. 3D: 40)** a first semiconductor layer having first and second ends and a central region that is thinner than the first and second ends **(FIG. 3D)**, the central region having first and second side surfaces extending upward from the substrate (col. 7, lines 42-66), epitaxially growing a semiconductor channel region **(FIG. 3G: 57 and FIG. 3I: 57A)** on at least one of the first and second side surfaces of the central region of the first semiconductor layer, a first side of the channel being exposed; removing the central region of the first semiconductor layer, thereby exposing a second side of the channel **(FIG. 3G)**; forming a dielectric layer **(FIG. 3H: 60)** on exposed surfaces of the semiconductor channel region; and forming a gate electrode **(FIG. 3I: 62)** on the dielectric layer (col. 8, lines 9-27).

In re claims 25-27, the use of a combination of Group IV elements or an alloy of silicon and Group IV element in forming the semiconductor channel region is well-known to one of ordinary skill in the art of making semiconductor devices.

In re claim 28, **Neudeck** discloses wherein the step of removing the first semiconductor layer does not appreciably remove the semiconductor region **(FIGS. 3D and 3G)**.

In re claim 29, **Neudeck** discloses wherein an etch stop is epitaxially grown between the first semiconductor layer and the semiconductor channel region **(FIG. 3E)**.

In re claim 30, **Neudeck** discloses wherein the method as recited in claim 14, wherein the gate electrode is formed of a material selected from the group consisting of polysilicon (col. 8, lines 8-27).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neudeck et al. (U.S. patent 5,273,921) as applied to claims 14-19, and 22-23 above.

In re claims 20 and 21, there is no evidence indicating the implanting step are critical and it has been held that it is not inventive to discover the optimum or workable range of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05. Note that the specification contains no disclosure

of either the critical nature of the claimed dimensions of any unexpected results arising there from. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (571) 272-1985. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.
February 3, 2004

W. DAVID COLEMAN
PRIMARY EXAMINER